Formulary - Advanced Computer Architecture (2024/2025)

This formulary has been made for the final exam. It might contain some mistakes or might be incomplete. However, this is what I bring to my exam, and maybe it can be useful for someone else.

Performance Metrics

Performance:

$$\text{Performance} = \frac{1}{\text{Execution Time}}$$

Relative Performance:

$$\begin{aligned}\text{Perf}(X) &= \left(1 + \tfrac{n}{100}\right) \times \text{Perf}(Y) \\ \text{ExecTime}(Y) &= \left(1 + \tfrac{n}{100}\right) \times \text{ExecTime}(X)\end{aligned}$$

Clock Frequency:

$$f_{CLK} = \frac{1}{T_{CLK}}$$

CPU Time

$$\text{CPU Time} = \text{IC} \times \text{CPI} \times T_{CLK}$$

Instruction Metrics

IPC:

$$\text{IPC} = \frac{1}{\text{CPI}}$$

Weighted Average CPI:

$$\begin{aligned}\text{CPI} &= \sum_{i=1}^{n} (\text{CPI}_i \times \text{F}_i) \\ \text{F}_i &= \frac{\text{I}_i}{\text{IC}}\end{aligned}$$

MIPS

Using clock frequency:

$$\text{MIPS} = \frac{f_{CLK}}{\text{CPI} \times 10^6}$$

Using execution time:

$$\text{MIPS} = \frac{\text{IC}}{\text{Execution Time} \times 10^6}$$

Memory Hierarchy

Average Memory Access Time (AMAT):

$$\text{AMAT} = \text{Hit Time} + \text{Miss Rate} \times \text{Miss Penalty}$$

Hierarchical (L1, L2) $\text{AMAT}_{\text{L1, L2}}$:

$$\begin{aligned}&\text{L1 Hit Time} + \text{L1 Miss Rate} \times \\ &(\\ &\quad \text{L2 Hit Time} + \\ &\quad \text{L2 Miss Rate} \times \text{L2 Miss Penalty} \\ &)\end{aligned}$$

Harvard Architecture $\text{AMAT}_{\text{Harvard}}$:

$$\begin{aligned}&(\%\text{Instr}) \times \\ &(\text{Hit Time} + \text{Miss Rate}_{\text{I\$}} \times \text{Miss Penalty}) + \\ &(\%\text{Data}) \times \\ &(\text{Hit Time} + \text{Miss Rate}_{\text{D\$}} \times \text{Miss Penalty})\end{aligned}$$

Pipeline Performance

Code efficiency:

$$\text{Code eff} = \frac{\text{IC}}{\#\text{ cycles} \times \#\text{ issues}}$$

Ideal CPI: $\text{CPI}_{ideal} = 1$

Realistic CPI:

$$\text{CPI} = 1 + \text{Stall Cycles per Instruction}$$

Clock Cycles:

$$\text{Clock Cycles} = \text{IC} + \text{Stall Cycles} + 4$$

CPI in pipeline:

$$\text{CPI} = \frac{\#\text{ Clock Cycles}}{\text{IC}}$$

MIPS in pipeline:

$$\text{MIPS} = \frac{f_{CLK}}{\text{CPI} \times 10^6}$$

Pipeline Speedup:

$$\text{Speedup}_{\text{pipeline}} = \frac{\text{Avg Exec Time Unpipelined}}{\text{Avg Exec Time Pipelined}}$$

Loops in Pipelines (k stalls, m instr. per iter)

Clock Cycles per iteration:

$$\text{Cycles}_{\text{iter}} = m + k + 4$$

CPI per iteration:

$$\text{CPI}_{\text{iter}} = \frac{m + k + 4}{m}$$

Asymptotic (n iterations):

$$\text{CPI}_{\infty=\text{AS}} = \frac{m + k}{m}$$

Amdahl's Law

Speedup:

$$\text{Speedup}(E) = \frac{1}{(1 - \text{F}) + \frac{\text{F}}{\text{S}}}$$

Maximum theoretical speedup:

$$\text{Speedup}_{\text{max}} = \frac{1}{1 - \text{F}}$$